MODERNIZATION OF U-70 GENERAL TIMING SYSTEM

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ABSTRACT

The paper outlines existing timing system of the IHEP accelerators complex (U-70) and the main goals of its modernization. Simplified structure of the new distributed General Timing System (GTS), its principal components and the timing network are described. Special attention is paid to reliability of the GTS operation, in particular to diagnostics of faults and malfunctions at the system. The developed means, ensuring the gradual transition from the old timing system to the new one, and the first results of the GTS operation during the accelerator last run are presented.

INTRODUCTION

The existing means of the IHEP accelerators timing were being created for each installation following the development of the Complex. As a result we have got a conglomerate of the different timing devices [1, 2, 3] with manual or computerized controls linked to each other by numerous and long cables. Such a situation and the lack of diagnostic means complicate the exploitation of the existing hardware and software. All that has required development of the new system, which have to have possibilities for autonomous and centralized timing, extended functionality, fully unified hardware, minimum quantity of the cables and module types, sufficient diagnostics, computerized controls and monitoring. The paper describes the solution of these tasks in the new GTS [4] of the IHEP accelerators complex.

The GTS distributes timing information (events and certain operational data) accompanied with 10KHz clock. The events support synchronization of both technological processes directly and control procedures through interrupt mechanism. The information is transported by means of encoded timing messages, using some sort of TDM method. The latter allows essential minimization of the cables number and unification of the hardware. For that purpose MIL1553 standard was chosen since its multidrop bus provides galvanic isolation from message receivers and keeps integrity if some of receivers are faulty. Besides that the choice in favor of this standard was done because it is widely used at the IHEP accelerators control system [5].

The timing message represents tandem of Command Word and Data Word (in terms of MIL1553 standard). Each Command Word carries event code and the clock pulse while the Data Word is foreseen for operational data (number of cycle, number of pulse-to-pulse modulation mode and others), which is necessary for the accelerators control system. All that information is packed into special format.

GTS STRUCTURE

Each of large installations (linac with booster, main accelerator and beam ejection system), situated in different remote buildings, has own timing message generator (TMG) (fig. 1). The latter supports autonomous timing during each start up period supplying local timing message receivers (TMR) with necessary timing information. All three TMG are linked with each other for global timing messages exchange in order to synchronize their operation. Thus all of them work as a distributed single source of timing messages.

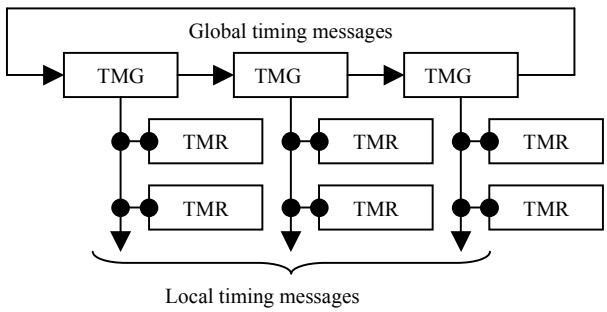

Figure 1: GTS simplified structure

Unlike MIL1553 conventional data traffic the GTS timing messages are propagated in one direction both at the global ring network and at the local radial one. The global messages are

transported between remote buildings through fiber optic cable (main line) or through low loss coaxial cable (reserve line). The local messages are delivered to each TMR by means of multidrop bus made of conventional MIL1553 twisted pair cable.

GTS MAIN COMPONENTS

Timing Message Generator (TMG)

The TMG acquires timing information from three sources:

- RAM with event codes defined for each local channel and being read by the corresponding local pulses;
- RAM with event codes programmed upon the time scale of the accelerator cycle and being read sequentially with the frequency of 10KHz;
- timing messages coming from global timing network (fig. 2).

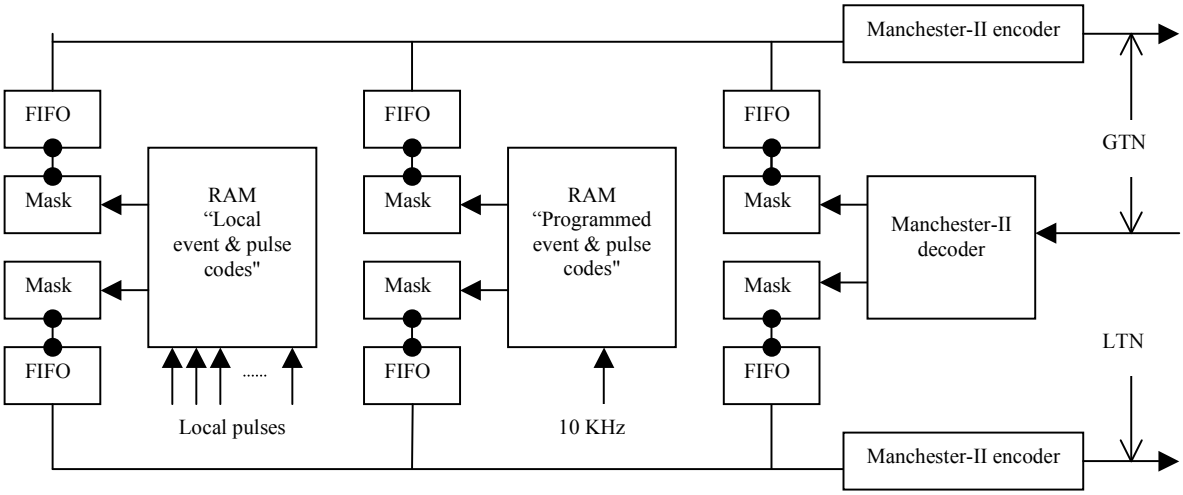

Figure 2: TMG simplified block-diagram

The TMG distributes the input information between global and local timing networks by means of masked gates [6]. The mask mechanism is also used to prevent non-stop circulation of global messages after each of them has completed one revolution.

The FIFO's provide smooth matching of the incoming and outcoming timing messages rates in the global (GTN) and local (LTN) timing networks. At the end of accelerator cycle the set of new codes are written down in Mask registers and in RAM's, then the 10KHz clock is restarted at the chosen moment.

Timing Message Receiver (TMR)

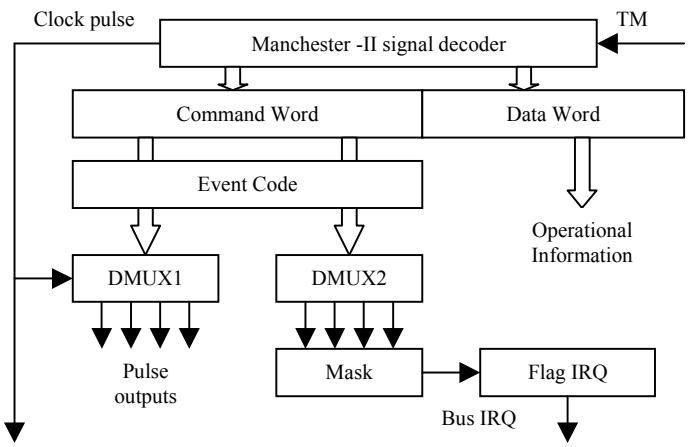

Figure 3: TMR simplified block-diagram

Each received serial timing message (TM) is converted by Manchester-II decoder into 16-bits Command and Data Words (fig. 3). The event code is transformed into pulse (synchronized with 10KHZ clock) at the corresponding output of the DMUX1 and into the DMUX2 output signal, which produce Interrupt Request (IRQ) having passed through the open masked gate. The mask register contents is written down in accordance with the task of the equipment controller. Its SBC software initiated by IRQ signal reads both Command Word and Data Word and then resets flag IRQ.

GTS DIAGNOSTICS

The timing system of the accelerators, especially cyclic ones, has to operate without any malfunctions since both the loss of a synchronization pulse and the appearance of any false pulse at inappropriate time can cause very heavy consequences. For fast localization of the failure the adequate diagnostic means are embedded at the GTS main components [7]. Part of them monitors constantly the timing messages stream in global and local timing networks while the others check the integrity of the TMR link with the GTS local multidrop bus and reliability of the TMR input timing information.

TM registration

The monitoring of the timing messages stream is executed by special device registering the TM codes and their time position within each accelerator cycle. The device contains two memory blocks – RAM1 and RAM2 (fig. 4). The TM codes are written in the RAM1 whereas the time of their appearance is written in second RAM. The time position data is prepared by Time Marks Counter, which operates with 5KHz frequency being started at the beginning of each accelerator cycle. Each incoming TM triggers Clock Generator (signal ST0) that produces control pulses. In their turn they write TM both words codes and current contents of Time Marks Counter in the corresponding blocks of memory, then increment the contents of the common Address Counter.

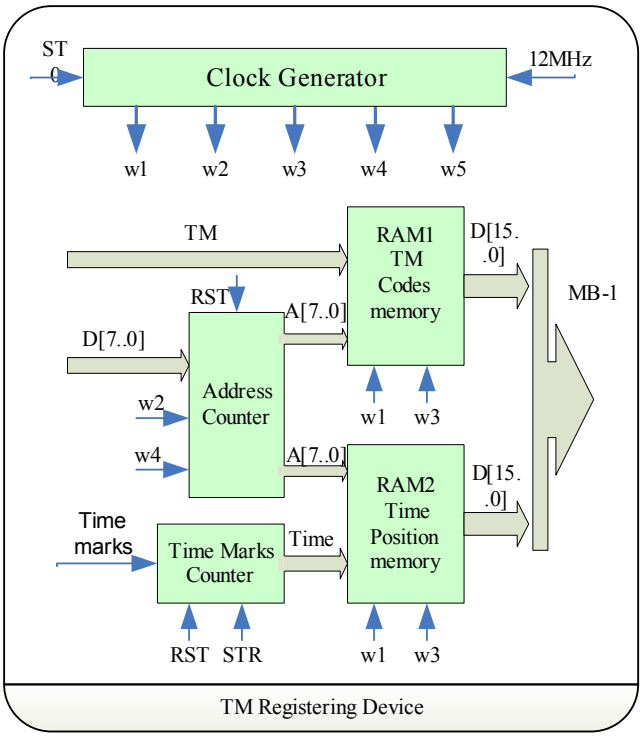

Figure 4: TM registering device functional diagram

At the end of accelerator cycle the stored data is transferred from the memory blocks to the Control System Data Base, both counters are reset, and then the Time Marks Counter is restarted. Single board computer (SBC) housed in the same crate as Registering Device executes all these actions.

These devices are built in all three TMG and are also installed at the end of each GTS local multidrop bus. As it was described, all of them are operating synchronously with the accelerator cycles and under guidance of the Control System means. But these rather simple devices have some limitations as the diagnostic tools. Firstly if the start signal is lost the device operation is interrupted till that signal appears again. Secondly the Registering Device cannot be efficiently used in the case of rare (but not less harmful) arbitrary malfunctions.

TM archiving

The efficient troubleshooting in these complicated cases needs the diagnostic tool to archive timing information during a long period and independently on external conditions. Such a tool with internal timing and essentially extended storage capacity was developed and produced. The tool is a portable autonomous device used where and when it is necessary. The device includes the following main blocks (fig.5):

- task administrator operating as a micro-program automat;
- energy-independent 32 Mb FLASH memory with limited number of rewriting cycles;
- energy-independent 64 Kb FRAM memory with unlimited number of rewriting cycles;
- memory dispatcher;
- RTC dispatcher;
- 32 bits counter incorporated in RTC (real time clock microchip).

The Task Administrator controls the device operation in accordance with the chosen task. There are three main tasks:

1. Storing timing messages in buffer FIFO memory during 10 s and archiving them in FLASH memory following certain algorithm;
2. Transferring stored information from FLASH memory to external computer;
3. Correcting the time setting in the RTC.

The task is selected and launched through the control program of the external computer. Switching on act initiates the first task.

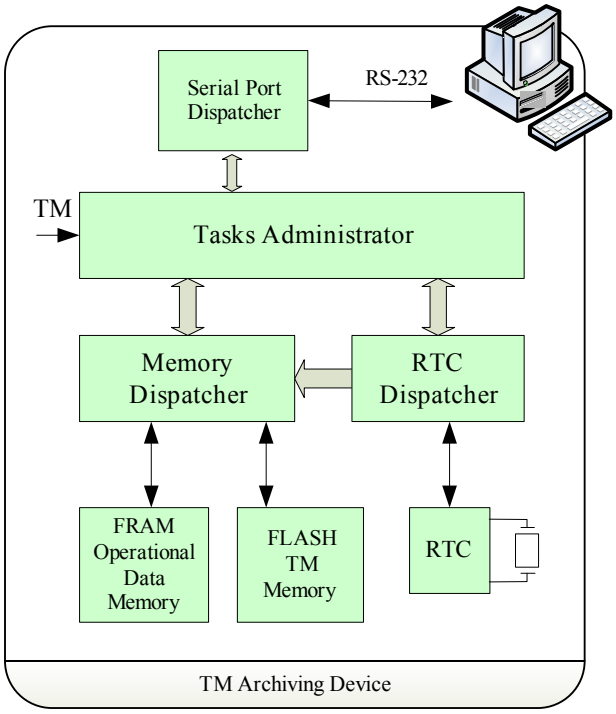

Figure 5: TM Archiving Device block-diagram

The Memory Dispatcher is filling data in the FLASH memory in some "endless ring mode to minimize the number of write/erase cycles for each cell and therefore to increase the memory resource. The size of FLASH memory allows storing the total number of timing messages circulating during four days of accelerator uninterrupted operation. Thus one can read and analyze the timing information got for the last four days.

The FRAM memory keeps the operational data such as micro-program codes of executed tasks, contents of the FLASH address counter, etc. In particular, each time after the new portion of timing information is transferred from the buffer FIFO to the FLASH memory the last contents of the FLASH address counter are written down in the FRAM memory.

The RTC Dispatcher supports protocol of interaction with RTC as well as forms current time data for the Memory Dispatcher. Unlike TM registering operation the archiving process is timed by internal clock and controlled by external computer what ensures its full functional autonomy.

Fault detection and alarm signalization

The data acquired from the above described diagnostic tools needs time for processing and working out the appropriate report for timing specialists. In order to warn operator about some simple faults (but not less serious) in good time the TM Registering Device outputs supplementary information not requiring any serious analysis:

- Overflow of Common Address Counter (there was abnormal number of TM);
- Overflow of Time Marks Counter (there was no counter restart);
- Zero state of Common Address Counter during the cycle (there was no any TM).

This information is written down in the device status register. The corresponding IRQ signal for the equipment controller SBC (EC SBC) initiates the transfer of the status register contents to the Control System upper level. The IRQ signal is produced either by dedicated timing event at the end of accelerator cycle or by the Counter overflow signal.

The TMR's plugged in the equipment controllers have diagnostic means, which execute permanent detection of input timing messages stream and parity check of both Command Word and Data Word. The first task is solved using regularity of the 10 KHz TM flow in the LTN. Any break in the flow creates IRQ signal for the EC SBC, which informs the Control System upper level of the fault. The MIL1553 protocol microchip used in the TMR module carries out the parity check, whose result is written down in status register of the module. Each incoming TM causes IRQ signal for SBC and thus initiates the transfer of the status register contents to the Control System upper level.

The computers of the accelerators Control System acquire the information of the faults and produce urgent alarm messages for operators. That computerized automatic GTS diagnostics is supplemented with LED indication of real time alarm signals on the timing modules front panels.

GTS PRESENT STATE

Now the overall functionality of the new GTS is covered by four types of the timing modules: timing network controller, memory for the programmed event codes, timing message encoder, timing message receiver. All these modules are made on the base of PLD or FPGA technology and in the Multibus-1 standard adopted for the IHEP accelerator control system [8]. The GTS software supporting the hardware settings and TM streams monitoring has been developed and debugged. The first GTS segment covering Linac and Booster was assembled and tested. The wide application of GTS diagnostic tools essentially simplified and accelerated the timing system commissioning. Thus that devices proved to be efficient means for GTS troubleshooting. The first GTS segment was put into operation in November - December of 2004 year and operated during all the accelerator run without any faults. On the contrary the Booster old timing system operation was accompanied with many problems. The rest of the system will be assembled and tested as a whole during the last months of this year.

Gradual transition from old timing systems to new GTS

In order to put the new GTS into operation without immediate changing the old application programs there was necessary to take into account two circumstances. Firstly the format of the old timing messages differs from the new one. Secondly for time crucial tasks the application software communicated directly with the registers of the old timing message receivers. Thus to avoid time consuming revision of old application software (at least temporary) for its adaptation to the new GTS a few hardware and software means have been prepared.

Modules simulating the old timing message receivers were developed and installed in the equipment controllers working with the old software (fig.6). The home-made multitask monitor VPV for the EC SBC was supplemented with certain options so as to work with the new GTS. These options allow using either new TMR with newly developed application software (ASW) or combination of the new TMR with the module-simulator for the existing (old) application programmes.

In the last case the monitor VPV having got IRQ signal from the new TMR reads Command Word and Data Word, then converts their codes in the old format and writes them in the corresponding registers of the simulating module. Thus the old software communicates with that module as with the old TMR. The last accelerator run fully confirmed the correctness of such an approach to the transition problem. Later on the old ASW will be rewritten for the new TMR and old TMR simulators will be removed from the eqipment controllers.

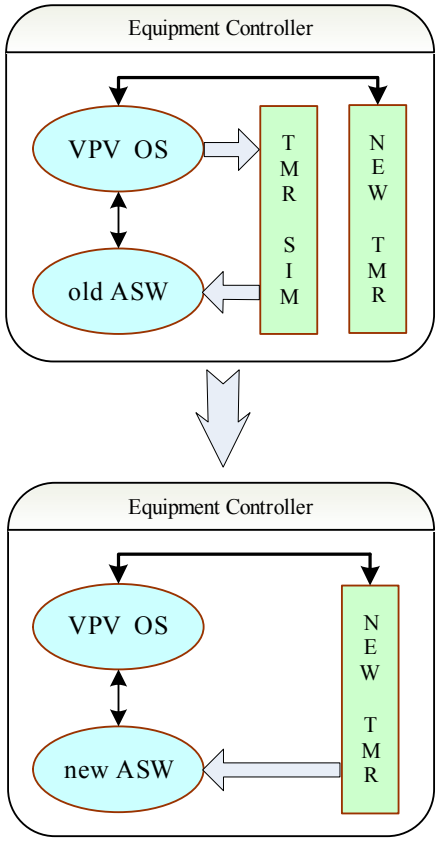

Figure 6: Transition to new GTS

Timing signals processing time

It is obvious that the timing signals processing such as Manchester encoding / decoding, the TM redistribution between the global and local networks, etc. retards the transportation of the timing information. The delay time between TMG input and output timing signals in different channels are as follows (μs):

- programmed events – 13.8;
- local events – 6.5 ± 1.1;
- global events – 52.8 ± 0.5.

The delay time between TMR input and output timing signals in different channels are as follows:

- channel “output pulses – 27.2 μs;
- channel “interrupt request (signal IRQ) – 45.2 μs.

The values of all these delays and their jitter are in the limits satisfying the requirements defined for U-70 GTS. The time of TM propagation along the cables is not taken into consideration since this time is comparatively small and its temperature fluctuations are negligible.

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